What is claimed is:

1. A method comprising:

determining whether execution of an instruction of a first thread may require a long latency; and

switching to a second thread if the instruction may require the long latency.

2. The method of claim 1, further comprising executing at least one additional instruction in the first thread while preparing to switch to the second thread.

3. The method of claim 1, wherein the determining is based on a stochastic analysis of whether the instruction will result in a long latency.

4. The method of claim 1, wherein the determining comprises applying the instruction to a lookup table in a processor pipeline.

5. The method of claim 4, further comprising providing a feedback signal from an instruction decoder to an instruction fetch unit to switch to the second thread.

6. The method of claim 1, wherein the long latency comprises less than ten processor cycles.

7. The method of claim 1, further comprising switching back to the first thread.

8. A method comprising:

switching from a first thread to a second thread if a condition that may result in a stall of a processor pipeline occurs during execution of the first thread in the processor pipeline.

9. The method of claim 8, further comprising determining whether the condition occurs by comparing an instruction to entries in a lookup table.

10. The method of claim 8, further comprising executing at least one additional instruction after the condition occurs and before switching to the second thread.

11. The method of claim 8, wherein the condition is based on a stochastic model.

12. The method of claim 8, further comprising providing a feedback signal from an instruction decoder to an instruction fetch unit to switch to the second thread.

13. An article comprising a machine-readable storage medium containing instructions that if executed enable a system to:

switch from a first thread to a second thread if a condition that may result in a stall of a processor pipeline occurs during execution of the first thread in the processor pipeline.

14. The article of claim 13, further comprising instructions that if executed enable the system to determine whether the condition occurs by comparing an instruction to entries in a lookup table.

15. The article of claim 13, further comprising instructions that if executed enable the system to execute at least one additional instruction in the first thread while the system prepares to switch to the second thread.

16. The article of claim 13, further comprising instructions that if executed enable the system to send a feedback signal to cause the switch from the first thread to the second thread.

17. An apparatus comprising:

a processor pipeline having a feedback loop to provide a feedback signal to cause the processor pipeline to switch

from a first thread to a second thread, the feedback signal to originate from a location in the processor pipeline before instruction execution.

18. The apparatus of claim 17, wherein the feedback signal is coupled between an instruction decoder and an instruction fetch unit.

19. The apparatus of claim 18, wherein the instruction decoder is coupled to provide the feedback signal to the instruction fetch unit when a predetermined condition occurs.

20. The apparatus of claim 19, wherein the instruction decoder includes logic to determine when the predetermined condition occurs.

21. The apparatus of claim 19, wherein the instruction decoder includes a lookup table that includes a list of predetermined conditions.

22. A system comprising:

a processor pipeline having a feedback loop to provide a feedback signal to cause the processor pipeline to switch from a first thread to a second thread, the feedback signal

to originate from a location in the processor pipeline before instruction execution; and

a wireless interface coupled to the processor pipeline.

23. The system of claim 22, further comprising at least one storage device to store code to enable the processor pipeline to switch from the first thread to the second thread if a predetermined condition occurs during execution of the first thread.

24. The system of claim 23, wherein the at least one storage device includes code to enable the processor pipeline to execute at least one additional instruction in the first thread while the system prepares to switch to the second thread.

25. The system of claim 22, wherein the feedback signal is coupled between an instruction decoder and an instruction fetch unit.

26. The system of claim 25, wherein the instruction decoder is coupled to provide the feedback signal to the instruction fetch unit when a predetermined condition occurs.

27. The system of claim 26, wherein the instruction decoder includes logic to determine when the predetermined condition occurs.

28. The system of claim 26, wherein the instruction decoder includes a lookup table that includes a list of predetermined conditions.

29. The system of claim 22, wherein the wireless interface comprises a dipole antenna.